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BSCpE 3A

**Asynchronous Binary Up Counter**

**VHDL Code:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.NUMERIC\_STD.ALL;

entity synbicount is

generic (

WIDTH : integer := 4 -- Change this to change counter size

);

port (

clk : in std\_logic;

reset : in std\_logic; -- Active-high synchronous reset

enable: in std\_logic;

count : out std\_logic\_vector(WIDTH-1 downto 0)

);

end entity synbicount;

architecture Behavioral of synbicount is

signal cnt\_reg : unsigned(WIDTH-1 downto 0);

begin

process(clk)

begin

if rising\_edge(clk) then

if reset = '1' then

cnt\_reg <= (others => '0');

elsif enable = '1' then

cnt\_reg <= cnt\_reg + 1;

end if;

end if;

end process;

count <= std\_logic\_vector(cnt\_reg);

end architecture Behavioral;